Performance Analysis of Symmetric and Asymmetric 4H-SiC Based Double Gate MOSFET

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Abstract: Silicon Carbide (SiC) has superior material properties such as higher breakdown field, thermal conductivity and wider bandgap which makes SiC promising alternative for various semiconductor applications. SiC occurs in crystalline structures or polytypes, having different properties of material. This paper presents 4H-SiC Double Gate MOSFET (DG MOSFET) in two forms, symmetric and asymmetric. The two designs were simulated for 22 nm, 40nm, 60 nm and 100 nm channel length. The results of both designs show better performance in terms of the leakage and switching characteristics.

Keywords: 4H-SiC, Semiconductor Devices, Double Gate MOSFET (DG MOSFET), Subthreshold Swing

Introduction

Silicon (Si) devices are used in majority of today's semiconductor based applications and with the advancement in technology, the necessity of rapid shrink in device size has increased so that more functions can be performed on a single chip [1]. The continual refinement have reached performance limitation of both material and device structure. The fast shrink in device dimension necessitates the integration of new device and this change requires either a better device design or better material. One such possibility are wide bandgap semiconductor material, such as Gallium Nitride (GaN), Diamond and Silicon Carbide (SiC) [2]. After many years of immense effort on the research of wide bandgap semiconductor device design and fabrication, processing techniques and material growth, electronic devices using SiC is finally starting to be commercialized and accepted by related industries. Wide bandgap devices commercial availability shows its improvement in electrical efficiency [3].

SiC is an attractive semiconductor to replaces Si because SiC have the potential to reduce energy losses. It has superior material properties such as high thermal conductivity, high field breakdown, wider bandgap and lower on-resistance [4]. The sensor based on SiC electronics can perform in the hostile conditions, where conventional Si based devices cannot function. The ability to perform at high power, high radiation and high temperature conditions makes SiC more reliable and appropriate option for variety of system and applications [5].

4H-SiC

SiC occurs in many different crystalline structures, which are referred as polytypes. The most common polytype used are 6H-SiC (α -SiC), 3C-SiC (β -SiC) and 4H-SiC. Among these 4H-SiC is an appropriate choice for device application having superior properties and advance technology [6]. It is the most commercially used SiC polytype which has the ability to grow a stable thermal oxide in the same way as that of Si. High thermal stability, low drift layer change and high switching speed are major benefits of it. The low on-resistance feature makes it more relevant for the high power applications [7]. It can also be operated for RF frequencies; it is figured out that SiC can achieve a ten-fold increase in power density at a given frequency. As 4H-SiC do not depend on conductivity modulation of the device, it is able to have low loss and high switching speed. Table 1 shows some important material properties of Si and 4H-SiC [8].

It has the advantage of having high critical field which in turn came out as high voltage majority carrier device. This results into low drift layer resistance two orders of magnitude lower than Si device [9]. The hurdle in the way of 4H-SiC is the interface traps which disrupt the device operation. However by controlling the temperature and gate biasing this can be handled to a great extent [10].

Apart from the above characteristics, 4H-SiC have high pressure and radiation resistance, high electron mobility and high stability to chemical reactions. For power devices it provides better electron transport properties. SiC Schottky diodes have already been manufactured and are commercially available. It has better switching characteristics and turn-on and turn-off losses have been reduced [11].

4H-SiC DG MOSFET

Scaling in the device dimensions raised the need of multi-gate device designs for more efficient performance. Double Gate MOSFET (DG MOSFET) is an example of this, which enables electrical coupling of the two gates, leading to a better gate control over the channel. The advantages of DG MOSFET include better subthreshold slope, volume inversion, threshold voltage and reduction in dopant fluctuations [12].

Fig. 1 represents the schematics of different types of DG MOSFET. There are two types of DG MOSFET symmetric and asymmetric DG MOSFET but it is further classified on the basis of voltage applied on gate terminal.

The voltage applied on the gate terminal induces charge in the channel between source and drain, which perform under the influence of electric field [13]. This determines the flow of current through the channel. Fig. 2(a) and Fig. 2(b) shows two mode of operation, switching both gates simultaneously (By interconnecting both gates and giving them one gate voltage) and switching at different voltages.

Device Design

For designing and simulations of device Cogenda Visual TCAD is used.

Design of symmetric 4H-SiC DG MOSFET

The proposed device design of symmetric 4H-SiC DG MOSFET consists of 4H-SiC substrate instead of Si. Gate material is n-polysilicon (N-poly) for both top gate and bottom gate. Table 2 shows material used for different regions of the device. Different channel lengths ranging from 22 nm to 100 nm are taken to analyze the effect of short channel and long channel length. The source and drain region are n-doped (ND = 1e+18 cm-3) with guassian doping profile and channel is p-doped (NA=1e+18 cm-3) with uniform doping profile.SiO2 is the gate dielectric and Aluminium (Al) is used for metal contact.

Design of asymmetric 4H-SiC DG MOSFET

The asymmetric configuration of the 4H-SiC DG MOSFET is similar to that of symmetric device design. But the gates have different materials so that there would be difference in work function of both gates. Oxide thickness is kept same for both top gate and bottom gate. Other parameters are same as that of symmetric device parameter.

Device Simulation and Analysis

Symmetric 4H-SiC DG MOSFET

The simulation is performed to obtain the output (Id versus Vgs curve) and (Id versus Vds curve) where former contain linear and logarithmic curves and latter have linear characteristics. The graphs for symmetric 4H-SiC DG MOSFET shows increment in drain current with channel length except for 40 nm where the increment is much higher than others as depicted in Fig. 3.

Fig. 4 shows drain current behavior for symmetric 4H-SiC DG MOSFET on various gate to source voltages Vg = 0.5 V, 0.6 V, 0.7 V, 0.8 V, 0.9 V, 1.0 V and channel lengths Lg = 22 nm, 40 nm, 60 nm and 100 nm. The drain voltage ranges from 0 - 2 V with step voltage of 0.05. It shows linear behavior of drain current with increase in the gate potential. Although after some time it attains saturation. This linear relation is a result of the fact that the device has short channel length, and hence the current becomes dependent on the saturation velocity instead of the mobility. The difference in the saturation value is very less for short channel length device designs as compared to the long channel length device designs.

Asymmetric 4H-SiC DG MOSFET

Fig. 5 shows the relationship between the drain current, Id, and the gate voltage, Vgs at different drain voltages for various channel lengths with logarithmic and linear configurations. The result shows that in asymmetric devices as the channel length gradually increases the drain current increases for 22 nm and 40 nm while it decreases for 60 nm and 100 nm.

Fig. 6 indicates Id - Vgs plots of 4H-SiC asymmetric DG MOSFET. It should be noted here that the relation between Id and Vg is not quadratic, but linear.

Table 2 presents the effect of channel length on performance parameters of symmetric 4H-SiC DG MOSFET and Table 3 represents the effect of channel length on performance parameters of asymmetric 4H-SiC DG MOSFET. For better performance of the device on-current should be more because it is an important aspect related to speed and off-current should be low to reduce the amount of power consumption.

Fig. 7 indicates the subthreshold swing for the channel lengths. It can be depicted that for asymmetric 4H-SiC DG MOSFET the subthreshold characteristics are better than that of symmetric 4H-SiC DG MOSFET.

Additionally, the subthreshold value is 60 mV/decade (which is the ideal value of subthreshold) for 60 nm and 100 nm swing.

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Conclusion

The two device designs presented in this paper, symmetric 4H-SiC DG MOSFET and asymmetric 4H-SiC DG MOSFET, represent significant improvements in the performance over conventional devices. Asymmetric 4H-SiC DG MOSFET has stable subthreshold behavior than symmetric 4H-SiC DG MOSFET. The simulated results shows that in the symmetric devices drain current reduces for applied voltages with gradual increase in channel length. While considering the asymmetric devices it shows decrement in drain current with channel length but both devices have very less leakage current. Thus SiC can come upon as the future electronics industry by replacing Si based devices.



(a) (b) Fig. 2 Different modes of operation of 4H-SiC DG MOSFET (a) Switching both gates simultaneously (b) Switching at different voltages

Parameters	Si	4H-SiC
Thermal conductivity	1.5W/cm	4.9 W/cm
Energy bandgap	1.12 eV	3.32 eV
Electron drift velocity	$1 \times 10^7 \mathrm{cm/s}$	2×10^7 cm/s
Breakdown electric field	2.5×10 ⁵ V/cm	2.2×10 ⁶ V/cm

Table 1 Si and 4H-SiC material properties

Table 2 Material used for different region symmetric 4H-SiC DG MOSFET

Region	Material
Gate	N-poly (n-polysilicon)
Gate oxide	Silicon Dioxide
Substrate	Silicon Carbide
Source/Drain (contact)	Aluminium



(a)



(b)



(c)





Fig. 3 Plot showing the transfer characteristics of symmetric 4H-SiC DG MOSFET at different lengths (a) 22nm (b) 40nm (c) 60nm (d) 100nm

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(b)



(c)



(d)

Fig. 4 I_d-V_{ds} plot for various gate voltages for symmetric 4H-SiC DG MOSFET at different channel lengths (a) 22nm (b) 40nm (c) 60nm (d) 100nm







(b)







Fig. 5 Plot showing the transfer characteristics of asymmetric 4H-SiC DG MOSFET at different lengths (a) 22nm (b) 40nm (c) 60nm (d) 100nm

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(b)



(c)



 $(d) \label{eq:generative} for a symmetric 4 H-SiC DG MOSFET at different channel lengths (a) 22nm (b) 40nm (c) 60nm$ (d) 100nm



Fig. 7 Subthreshold swing versus channel length

Table 3 Simulated results of asymmetric 4H-SiC DG MOSFET device performance parameters with channel lengths

Channel length	Parameters			
	I _{on} (A)	$J_{\text{off}}(A)$	Ion/ Laff	
22 nm	1.47e ⁻⁰⁴	5.56e ⁻⁰⁹	3×10 ⁸	
40 nm	2.65e ⁻⁰⁴	5.67e ⁻⁰⁸	2×10 ⁸	
60 nm	2.54e ⁻⁰⁴	8.71e ⁻¹¹	1×10 ⁸	
100 nm	2.27e-04	3.34e ⁻¹⁰	1×10 ⁸	

References

- Srivastava, V. M.; Kapoor, S.; Nitasha, Jaswal, N.; Singh, G.: Full Subtractor Circuit Design with Independent Double Gate Transistor. In: International Conference on Recent Trends in Information, Telecommunication and Computing held in Kochi, India, ITC.2010.25, 12-13 March 2010.
- [2] Hariharan, V.; Thakker, R.; Singh, K.; Sachid, A. B.; Patil, M. B.; Vasi, J.; Rao, V. R.: Drain current model for nanoscale double-gate MOSFETs. Solid-State Electronics, 53(9), 1001-1008 (2009).
- [3] Alok, D.; Arnold, E.; Egloff, R.; Barone, J.; Murphy, J.; Conrad, R.; Burke, J.: 4H-SiC RF Power MOSFETs. Electron Devices, 22(12), 577 – 578 (2001).
- [4] Nakamura, T.; Aketa, M.; Nakano, Y.; Sasagawa, M.; Otsuka, T.: Novel Developments Towards Increased SiC Power Device and Module Efficiency. In: IEEE Conference on EnergyTech held in Cleveland, Ohio, EnergyTech.2012.6304633, 29-31 May 2012.
- [5] Bhatnagar, M.; Baliga, B. J.: Comparison of 6H-SiC, 3C-SiC, and Si for Power Devices. Electron Devices, vol. 40(3), 645-655 (1993).
- [6] Kimoto, T.; Yoshioka, H.; Nakamura, T.: Physics of SiC MOS Interface and Development of Trench MOSFETs. In: IEEE Conference on Wide Bandgap Power Devices and Applications (WiPDA) held in Columbus, Ohio, WiPDA.2013.6695580, 27-29 October 2013.
- [7] Zolper, J. C.: Emerging Silicon Carbide Power Electronics Components. In: IEEE Twentieth Annual Conference on Applied Power Electronics (APEC) held in Austin, Texas, APEC.2005.1452877, 6-10 March 2005.
- [8] Stevanovic, L. D.; Matocha, K. S.; Losee, P. A.; Glaser, J. S.; Nasadoski, J.; Arthur, S. D.: Recent Advances in Silicon Carbide MOSFET Power Devices. In: IEEE Twenty-Fifth Annual Conference on Applied Power Electronics (APEC) held in Palm Springs, California, APEC.2010.5433640, 21-25 February 2010.
- [9] Ryu, S.; Krishnaswami, S.; Hull, B.; Richmond, J.; Agarwal, A.; Hefner, A.: 10 kV, 5A 411-SiC Power DMOSFET. In: IEEE 18th International Symposium on Power Semiconductor Devices & IC's held in Naples, Italy, ISPSD.2006.1666122, 4-8 June 2006.
- [10] Potbhare, S., Goldsman, N., Lelis, A., McGarrity, J. M., McLean, F. B. and Habersat, D.: A Physical Model of High Temperature 4H-SiC MOSFETs. Electron Devices, 55 (8), 2029 – 2040 (2008).
- [11] Han, J.; Kim, C.; Choi, Y.: Universal Potential Model in Tied and Separated Double-Gate MOSFETs with Consideration of Symmetric and Asymmetric Structure. Electron Devices, 55 (6),1472-1479 (2008).
- [12] Ferney, A.; Chaves.; Jimenez, D.; Francisco, J.; Ruiz, G.; Godoy, A.; Sune, J.: Accurate Calculation of Gate Tunneling Current in Double-Gate and Single-Gate SOI MOSFETs Through Gate Dielectric Stacks. Electron Devices, 59 (10), 2589 – 2595 (2012).
- [13] Pucknell, A. D.; Eshraghian, K.: Basic VLSI Design. PHI, New Delhi (1994).